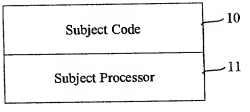

Fig. 1

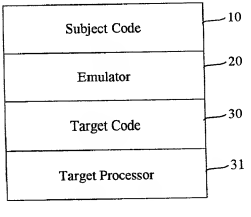

Fig. 2

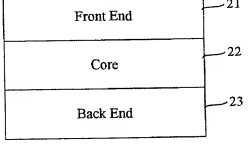

Fig. 3

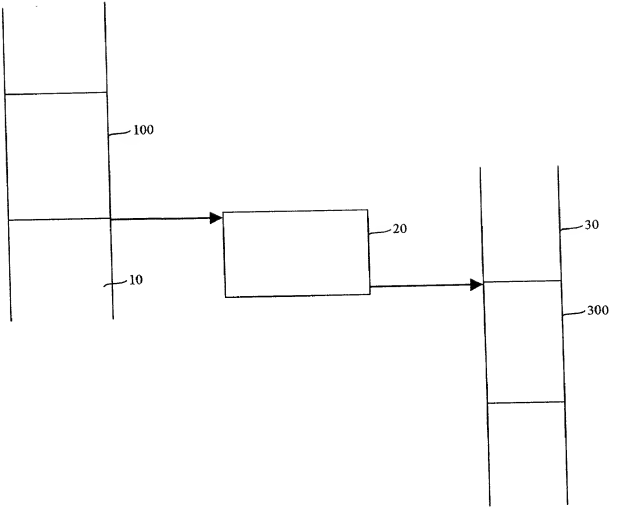

Fig. 4

Register Memory Map

Register	Target Set A Values	Target Set B Values
Reg X	Reg X_A Definitive	Reg X_B Speculative
Reg Y	Reg Y_A Definitive	Reg Y_B Speculative
...	...	...

Fig. 5

Register Memory Map

Register	Target Set A Values	Target Set B Values
Reg X	Reg X_A Definitive	Reg X_B Speculative
Reg Y	Reg Y_A Speculative	Reg Y_B Definitive
...		...

Fig. 6